What is claimed is:

1. A debugging apparatus comprising:

a processor core operated by a program stored in a program memory to read a data stored in a data memory or write a data;

a debugger controller for performing a debugging on the processor core upon receipt of a command from a host computer and outputting a data break point address; and

a memory break controller for observing an address of a data memory used by the processor core, recognizing an address as a break point address to output a break signal to the debugger controller and the processor core to suspend the operation of the processor core, when the address is sensed to be identical, and transmitting a corresponding address and data to the host computer through the debugger controller.

2. The apparatus of claim 1, wherein the data memory stores a data value outputted from the processor core.

3. The apparatus of claim 1, wherein the memory break controller transmits an address and a data recognized as a break point, activates an operation of the processor core, and outputs the used address and the data of the data memory to the host computer through the debugger controller until a break signal is outputted again.

4. The apparatus of claim 3, wherein the host computer recognizes a

data flow and change by the address and the data outputted from the memory break controller.

5. The apparatus of claim 1, wherein the memory break controller comprises:

a memory break control register being activated by the break point address and the control signal inputted from the debugger controller;

an address register for storing the break point address inputted from the memory break control register;

an address comparator for comparing the address of the data memory currently used by the processor core and the break point address stored in the address register;

a data register for storing the data of the break point address stored in the address register; and

a data comparator for comparing the data of the current address outputted from the data memory and the data of the break point address stored in the data register.

6. The apparatus of claim 5, wherein the memory break control register comprises:

a memory break enable flag for activating the memory break controller;

a data check flag for sensing an address of the data memory which is identical to the break point address stored in the address register, and being enabled when the content of the data of the sensed address is outputted; and

an address trace check flag for being enabled when the content of the

address of the data memory which is identical to the break point address stored in the address register is outputted.

7. The apparatus of claim 6, wherein when the address trace check flag is enabled, it outputs addresses and data of every memory which are read from or written in the processor core before the content of the break address is updated.

8. A debugging apparatus for informing a data transition state, comprising:

a debugger controller for outputting a control signal for performing a debugging, a memory break point address, and a break enable signal;

a processor core being activated by the control signal outputted from the debugger controller, and reading a data stored in a data memory or writing a data;

a memory break control register being activated by the break point address and the control signal inputted from the debugger controller;

an address register for storing the break point address inputted from the memory break control register;

an address comparator for comparing the address of the data memory which is currently used by the processor and the break point address stored in the address register;

a data register for storing the data of the break point address stored in the address register; and

a data comparator for comparing the data of the current address outputted from the data memory and the data of the break point address stored in the data

register.

9. A debugging method comprising the steps of:

outputting an address of a data memory to be observed, that is a break point address and a break enable signal, when a processor is switched to a debugging mode;

storing the outputted break point address, and operating the processor in a general operation state;

comparing the stored break point address and the address of the data memory currently used by the processor core, while the process is being operated;

outputting a break signal to suspend the process core, if the address of the data memory currently used by the processor core and the stored break point address are identical to each other; and

suspending the processor core by the outputted break signal and switching the processor to a debugging mode to debug the program.

10. The method of claim 9, wherein in the step of operating a processor, a memory break enable flag of a memory break controller is enabled according to an outputted break enable signal, and a data check flag and an address check flag are disabled, in order to initialize the processor, and then the break point address is stored.

11. The method of claim 9, wherein the step of outputting a break signal comprises:

a step in which when an address of the data memory currently used by the processor core and the stored break point address are identical to each other, it is determined whether the processor reads the data stored in the corresponding address or writes a data;

a step in which, in case of reading a data, the address trace check flag and the data check flag of the memory break control register are enabled;

a step in which the corresponding address of the data memory and the stored break point address are compared again; and

a step in which, if the corresponding address of the data memory and the break point address are not identical to each other, the corresponding address and data of the data memory are transmitted to the host computer.

12. The method of claim 11, wherein the step of comparing address comprises:

a step in which, if the corresponding address of the data memory and the break point address are identical to each other, it is determined whether the processor reads a data stored in the data memory of the corresponding address or writes a data in the data memory of the corresponding address; and

a step in which, in case of writing a data, the data check flag of the memory break controller is enabled and a break signal for suspending the processor core is outputted.

13. The method of claim 12, wherein, in case of reading a data upon judgement, an address of the next data memory to be used by the processor core and the break point address are compared.

14. The method of claim 11, wherein, in case of writing a data in the judging step, the data check flag of the memory break controller is set and the operation of the processor core is discontinued.

15. The method of claim 9, wherein, in the step of outputting a break signal, when the operation of the processor core is suspended by the break signal, the address and data of the corresponding data memory are transmitted, and then the operation of the processor core is activated to output an address and a data of the data memory used by the processor core until a break signal is outputted again.

16. A debugging method for informing a data transition state, comprising:

a step in which when a processor is switched into a debugging mode, an address of a data memory to be observed, that is, a break point address, and a break enable signal are outputted;

a step in which the outputted break point address is stored;

a step in which the stored break point address and an address of a data memory currently used by a processor core are compared;

a step in which, when the address of the data memory currently used by the processor core and the stored break point address are identical to each other, it is determined whether the processor core reads a data stored in the corresponding address or writes a data;

a step in which, in case of writing a data in a corresponding address, a data check flag of a memory break controller is enabled and a break signal for

suspending the processor core is outputted;

a step in which, when the processor core is suspended by the outputted break signal, the address and the data of the corresponding data memory are outputted; and

a step in which the operation of the processor core is activated and the address and the data of the data memory used by the processor are outputted until a break signal is outputted again.

17. The method of claim 16, wherein, in case of reading a data upon judgement, an address of the next data memory used by the processor core and the break point address are compared.